FDP4N60NZ / FDPF4N60NZ
N-Channel MOSFET
600V, 3.8A, 2.5Ω

Features
- \( R_{DS(on)} = 1.9Ω \) (Typ.)@ \( V_{GS} = 10V, I_D = 1.9A \)
- Low Gate Charge (Typ. 8.3nC)
- Low \( C_{rss} \) (Typ. 3.7pF)
- Fast Switching
- 100% Avalanche Tested
- Improved \( dv/dt \) Capability
- RoHS Compliant

Description
These N-Channel enhancement mode power field effect transistors are produced using Fairchild’s proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.

MOSFET Maximum Ratings \( T_C = 25^\circ C \) unless otherwise noted*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>FDP4N60NZ</th>
<th>FDPF4N60NZ</th>
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<tr>
<td>( V_{DSS} )</td>
<td>Drain to Source Voltage</td>
<td>600</td>
<td>V</td>
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</tr>
<tr>
<td>( V_{GSS} )</td>
<td>Gate to Source Voltage</td>
<td>±25</td>
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<td></td>
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<tr>
<td>( I_D )</td>
<td>Drain Current</td>
<td>3.8</td>
<td>3.8*</td>
<td>A</td>
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<tr>
<td>( I_{DM} )</td>
<td>Drain Current</td>
<td>2.3</td>
<td>2.3*</td>
<td>A</td>
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<tr>
<td>( E_{AS} )</td>
<td>Single Pulsed Avalanche Energy</td>
<td>223.8</td>
<td>mJ</td>
<td></td>
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<tr>
<td>( I_{AR} )</td>
<td>Avalanche Current</td>
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<td>A</td>
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<tr>
<td>( E_{AR} )</td>
<td>Repetitive Avalanche Energy</td>
<td>8.9</td>
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<td>( dv/dt )</td>
<td>Peak Diode Recovery dv/dt</td>
<td>10</td>
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<tr>
<td>( P_D )</td>
<td>Power Dissipation</td>
<td>89</td>
<td>28</td>
<td>W</td>
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<tr>
<td>( T_J, T_{STG} )</td>
<td>Operating and Storage Temperature Range</td>
<td>-55 to +150</td>
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<tr>
<td>( T_L )</td>
<td>Maximum Lead Temperature for Soldering Purpose, 1/8&quot; from Case for 5 Seconds</td>
<td>300</td>
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*Drain current limited by maximum junction temperature

Thermal Characteristics

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<td>( R_{JC} )</td>
<td>Thermal Resistance, Junction to Case</td>
<td>1.4</td>
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<td>( R_{CS} )</td>
<td>Thermal Resistance, Case to Sink Typ</td>
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<td>( R_{JA} )</td>
<td>Thermal Resistance, Junction to Ambient</td>
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## Package Marking and Ordering Information

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## Electrical Characteristics

**TC** = 25°C unless otherwise noted

### Off Characteristics

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<th>Max.</th>
<th>Units</th>
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<td>BVDS</td>
<td>Drain to Source Breakdown Voltage</td>
<td>I_D = 250µA, V_GS = 0V, TC = 25°C</td>
<td>600</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>ΔBVoss</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>I_D = 250µA, Referenced to 26°C</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
<td>V/ºC</td>
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<tr>
<td>IDSS</td>
<td>Zero Gate Voltage Drain Current</td>
<td>V_DS = 600V, V_GS = 0V</td>
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<td>-</td>
<td>1</td>
<td>µA</td>
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<tr>
<td>IGSS</td>
<td>Gate to Body Leakage Current</td>
<td>V_GS = ±25V, V_DS = 0V</td>
<td>-</td>
<td>-</td>
<td>±10</td>
<td>µA</td>
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### On Characteristics

<table>
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<td>VGSH</td>
<td>Gate Threshold Voltage</td>
<td>V_GS = V_DS, I_D = 250µA</td>
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<td>5.0</td>
<td>V</td>
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<td>RDS(on)</td>
<td>Static Drain to Source On Resistance</td>
<td>V_GS = 10V, I_D = 1.9A</td>
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<td>1.9</td>
<td>2.5</td>
<td>Ω</td>
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<td>gFS</td>
<td>Forward Transconductance</td>
<td>V_DS = 20V, I_D = 1.9A</td>
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### Dynamic Characteristics

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<th>Max.</th>
<th>Units</th>
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<tr>
<td>Ciss</td>
<td>Input Capacitance</td>
<td>V_DS = 25V, V_GS = 0V, f = 1MHz</td>
<td>-</td>
<td>385</td>
<td>510</td>
<td>pF</td>
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<td>Coss</td>
<td>Output Capacitance</td>
<td></td>
<td>-</td>
<td>40</td>
<td>60</td>
<td>pF</td>
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<tr>
<td>Crss</td>
<td>Reverse Transfer Capacitance</td>
<td></td>
<td>-</td>
<td>3.7</td>
<td>5</td>
<td>pF</td>
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<tr>
<td>Qgs(tot)</td>
<td>Total Gate Charge at 10V</td>
<td>V_DS = 480V, I_D = 3.8A</td>
<td>-</td>
<td>8.3</td>
<td>10.8</td>
<td>nC</td>
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<tr>
<td>Qgs</td>
<td>Gate to Source Gate Charge</td>
<td>V_DS = 10V</td>
<td>-</td>
<td>2.1</td>
<td>-</td>
<td>nC</td>
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<td>Qgd</td>
<td>Gate to Drain “Miller” Charge</td>
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<td>-</td>
<td>3.3</td>
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### Switching Characteristics

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<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
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<tr>
<td>t(on)</td>
<td>Turn-On Delay Time</td>
<td>V_DD = 300V, I_D = 3.8A</td>
<td>-</td>
<td>12.7</td>
<td>35.4</td>
<td>ns</td>
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<tr>
<td>t_r</td>
<td>Turn-On Rise Time</td>
<td>R_G = 25Ω</td>
<td>-</td>
<td>15.1</td>
<td>40.2</td>
<td>ns</td>
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<tr>
<td>t(off)</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>-</td>
<td>30.2</td>
<td>70.4</td>
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<tr>
<td>t_f</td>
<td>Turn-Off Fall Time</td>
<td></td>
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<td>12.8</td>
<td>35.6</td>
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### Drain-Source Diode Characteristics

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<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
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<td>ISD</td>
<td>Maximum Continuous Drain to Source Diode Forward Current</td>
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<td>A</td>
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<tr>
<td>IDM</td>
<td>Maximum Pulsed Drain to Source Diode Forward Current</td>
<td></td>
<td>-</td>
<td></td>
<td>15</td>
<td>A</td>
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<tr>
<td>VGS</td>
<td>Drain to Source Diode Forward Voltage</td>
<td>V_GS = 0V, I_SD = 3.8A</td>
<td>-</td>
<td></td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>t_r</td>
<td>Reverse Recovery Time</td>
<td>V_GS = 0V, I_SD = 3.8A, dt/dt = 100A/µs</td>
<td>-</td>
<td>168</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Qrr</td>
<td>Reverse Recovery Charge</td>
<td></td>
<td>-</td>
<td>0.7</td>
<td>-</td>
<td>µC</td>
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</table>

**Notes:**
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 31mH, I_GS = 3.8A, V_DD = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_SD ≤ 3.8A, dI/dt ≤ 200A/µs, V_DD ≤ BV_DS, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300µs, Dual Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics
Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

- $V_{GS} = 10.0V$
- $6.0V$
- $7.0V$
- $6.5V$
- $6.0V$
- $5.5V$

*Notes:*
1. 250μs Pulse Test
2. TC = 25°C

**Figure 2. Transfer Characteristics**

*Notes:*
1. $V_{DS} = 20V$
2. 250μs Pulse Test

**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

- $V_{GS} = 10V$
- $V_{GS} = 20V$

*Note: TC = 25°C*

**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

*Notes:*
1. $V_{GS} = 0V$
2. 250μs Pulse Test

**Figure 5. Capacitance Characteristics**

**Figure 6. Gate Charge Characteristics**

*Note:*
1. $V_{GS} = 0V$
2. $f = 1MHz$

*Coss = Cgs + Cgd  (Cds = shorted)  
Ciss = Cds + Cgd  
Crss = Cgd*
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

![Breakdown Voltage Variation Graph]

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 250 \mu A$

Figure 8. On-Resistance Variation vs. Temperature

![On-Resistance Variation Graph]

*Notes:
1. $V_{GS} = 10V$
2. $I_D = 1.9A$

Figure 9. Maximum Safe Operating Area vs. Case Temperature

![Maximum Safe Operating Area Graph]

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 250 \mu A$

Figure 10. Maximum Drain Current

![Maximum Drain Current Graph]

*Notes:
1. $V_{GS} = 10V$
2. $I_D = 1.9A$

Figure 11. Unclamped Inductive Switching Capability

![Unclamped Inductive Switching Capability Graph]

*Notes:
1. $T_C = 25^\circ C$
2. $T_J = 125^\circ C$

$R_{\theta JC} = 4.5^\circ C/W$

$V_{GS} = 10V$

$R_{\omega} = 4.5^\circ C/W$

$I_{D}, \text{ Drain Current [A]}

$T_J, \text{ Junction Temperature} [\circ C]$

$V_{DS}, \text{ Drain-Source Voltage [V]$

Operation in This Area is Limited by $R_{\theta JC}$

$T_J = 25^\circ C$

$t_{AV}, \text{ TIME IN AVALANCHE (ms)}$

$I_{AS}, \text{ AVALANCHE CURRENT (A)}$

$t_{AV} \times \text{ TIME IN AVALANCHE (ms)}$

$t_{AV} = 0.01 \times 1$

$I_{AS} = 0.01 \times 1$
Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

*Notes:
1. $Z_{\theta JC}(t) = 4.5^\circ C/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} \cdot Z_{\theta JC}(t)$
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

\[ E_{AS} = \frac{1}{2} L_{AS} I_d(t)^2 \]
Peak Diode Recovery dv/dt Test Circuit & Waveforms

- DUT
- \( V_{DS} \)
- \( I_{SD} \)
- Driver
- Same Type as DUT
- \( V_{GS} \) controlled by \( R_G \)
- \( I_{SD} \) controlled by pulse period

\[ V_{GS} \] (Driver) \[ \frac{D}{10V} \] (Gate Pulse Width) \[ \frac{1}{Gate Pulse Period} \]

\[ I_{SD} \] (DUT) \[ \frac{I_{RM}}{di/dt} \] (Body Diode Forward Current)

\[ V_{DS} \] (DUT) \[ V_{SD} \] (Body Diode Reverse Current)

Body Diode Recovery dv/dt

Body Diode Forward Voltage Drop
Package Dimensions

TO-220

NOTES:

A) CONFORMS TO JEDEC TO-220
VARIATION AB EXCEPT WHERE NOTED
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Dimensions in Millimeters
Package Dimensions

TO-220F

* Front/Back Side Isolation Voltage : AC 2500V

Dimensions in Millimeters
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<th>Product Status</th>
<th>Definition</th>
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<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
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<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
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<tr>
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<td>Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.</td>
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