Description
The AFBR-5800Z family of transceivers from Agilent provide the system designer with products to implement a range of Fast Ethernet, FDDI and ATM (Asynchronous Transfer Mode) designs at the 100 Mb/s-125 MBd rate.

The transceivers are all supplied in the industry standard 1 x 9 SIP package style with either a duplex SC or a duplex ST* connector interface.

FDDI PMD, ATM and Fast Ethernet
2 km Backbone Links
The AFBR-5803Z/5803TZ are 1300 nm products with optical performance compliant with the FDDI PMD standard. The FDDI PMD standard is ISO/IEC 9314-3: 1990 and ANSI X3.166 - 1990.

These transceivers for 2 km multimode fiber backbones are supplied in the small 1 x 9 duplex SC or ST package style.

The AFBR-5803Z/5803TZ is useful for both ATM 100 Mb/s interfaces and Fast Ethernet 100 Base-FX interfaces. The ATM Forum User-Network Interface (UNI) Standard, Version 3.0, defines the Physical Layer for 100 Mb/s Multimode Fiber Interface for ATM in Section 2.3 to be the FDDI PMD Standard. Likewise, the Fast Ethernet Alliance defines the Physical Layer for 100 Base-FX for Fast Ethernet to be the FDDI PMD Standard.

ATM applications for physical layers other than 100 Mb/s Multimode Fiber Interface are supported by Agilent. Products are available for both the single mode and the multimode fiber SONET OC-3c (STS-3c) ATM interfaces and the 155 Mb/s-194 MBd multimode fiber ATM interface as specified in the ATM Forum UNI.

Contact your Agilent sales representative for information on these alternative Fast Ethernet, FDDI and ATM products.

Features
- Full compliance with the optical performance requirements of the FDDI PMD standard
- Full compliance with the FDDI LCF-PMD standard
- Full compliance with the optical performance requirements of the ATM 100 Mb/s physical layer
- Full compliance with the optical performance requirements of 100 Base-FX version of IEEE 802.3u
- Multisourced 1 x 9 package style with choice of duplex SC or duplex ST* receptacle
- Wave solder and aqueous wash process compatible
- Single +3.3 V or +5 V power supply
- RoHS Compliance

Applications
- Multimode fiber backbone links
- Multimode fiber wiring closet to desktop links
- Very low cost multimode fiber links from wiring closet to desktop
- Multimode fiber media converters

*ST is a registered trademark of AT&T Lightguide Cable Connectors.
**Transmitter Sections**

The transmitter section of the AFBR-5803Z and AFBR-5805Z series utilize 1300 nm Surface Emitting InGaAsP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V or +5 V supply, into an analog LED drive current.

**Receiver Sections**

The receiver sections of the AFBR-5803Z and AFBR-5805Z series utilize InGaAs PIN photodiodes coupled to a custom silicon transimpedance preamplifier IC. These are packaged in the optical subassembly portion of the receiver.

These PIN/preamplifier combinations are coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. The data output is differential. The signal detect output is single-ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a +3.3 V or +5 V power supply.

**Package**

The overall package concept for the Agilent transceivers consists of the following basic elements; two optical subassemblies, an electrical subassembly and the housing as illustrated in Figure 1 and Figure 1a.

The package outline drawings and pin out are shown in Figures 2, 2a and 3. The details of this package outline and pin out are compliant with the multisource definition of the 1 x 9 SIP. The low profile of the Agilent transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

The optical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC chips and various surface-mounted passive circuit elements are attached.

The package includes internal shields for the electrical and optical subassemblies to ensure low EMI emissions and high immunity to external EMI fields.

The outer housing including the duplex SC connector receptacle or the duplex ST ports is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Agilent design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with duplex or simplex SC or ST connector fiber cables.
Figure 1a. ST Connector Block Diagram.

Figure 2. SC Connector Package Outline Drawing with standard height.

Note 1: Phosphor bronze is the base material for the posts & pins. For lead-free soldering, the solder posts have Tin Copper over Nickel plating, and the electrical pins have pure Tin over Nickel plating.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

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Note: Phosphor bronze is the base material for the posts & pins. For lead-free soldering, the solder posts have Tin Copper over Nickel plating, and the electrical pins have pure Tin over Nickel plating.
Figure 2a. ST Connector Package Outline Drawing with standard height.

**Note 1:** Phosphor bronze is the base material for the posts & pins. For lead-free soldering, the solder posts have Tin Copper over Nickel plating, and the electrical pins have pure Tin over Nickel plating.

**DIMENSIONS IN MILLIMETERS (INCHES).**

Figure 2a. ST Connector Package Outline Drawing with standard height.

**Figure 3. Pin Out Diagram.**
**Application Information**

The Applications Engineering group in the Agilent Fiber Optics Communication Division is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Agilent sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

**Transceiver Optical Power Budget versus Link Length**

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transceiver series specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 µm and 50/125 µm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Agilent LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The Agilent 1300 nm LEDs will experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Agilent sales representative for additional details.

Figure 4 was generated with an Agilent fiber optic link model containing the current industry conventions for fiber cable specifications and the FDDI PMD and LCF-PMD optical parameters. These parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI X3T9.5 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

When used in Fast Ethernet, FDDI and ATM 100 Mb/s applications the performance of the 1300 nm transceivers is guaranteed over the signaling rate of 10 MBd to 125 MBd to the full conditions listed in individual product specification tables.
The Agilent 1300 nm transceivers are designed to operate per the system jitter allocations stated in Tables E1 of Annexes E of the FDDI PMD and LCF-PMD standards.

The Agilent 1300 nm transmitters will tolerate the worst case input electrical jitter allowed in these tables without violating the worst case output jitter requirements of Sections 8.1 Active Output Interface of the FDDI PMD and LCF-PMD standards.

The Agilent 1300 nm receivers will tolerate the worst case input optical jitter allowed in Sections 8.2 Active Input Interface of the FDDI PMD and LCF-PMD standards without violating the worst case output electrical jitter allowed in the Tables E1 of the Annexes E.

The jitter specifications stated in the following 1300 nm transceiver specification tables are derived from the values in Tables E1 of Annexes E. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex E allocation example. In practice the typical contribution of the Agilent transceivers is well below these maximum allowed amounts.

**Recommended Handling Precautions**

Agilent recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The AFBR-5800 series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

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**Transceiver Jitter Performance**

The Agilent 1300 nm transceivers are designed to operate per the system jitter allocations stated in Tables E1 of Annexes E of the FDDI PMD and LCF-PMD standards.

The Agilent 1300 nm transmitters will tolerate the worst case input electrical jitter allowed in these tables without violating the worst case output jitter requirements of Sections 8.1 Active Output Interface of the FDDI PMD and LCF-PMD standards.

The Agilent 1300 nm receivers will tolerate the worst case input optical jitter allowed in Sections 8.2 Active Input Interface of the FDDI PMD and LCF-PMD standards without violating the worst case output electrical jitter allowed in the Tables E1 of the Annexes E.

The jitter specifications stated in the following 1300 nm transceiver specification tables are derived from the values in Tables E1 of Annexes E. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex E allocation example. In practice the typical contribution of the Agilent transceivers is well below these maximum allowed amounts.

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Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.
**Solder and Wash Process Compatibility**

The transceivers are delivered with protective process plugs inserted into the duplex SC or duplex ST connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

**Shipping Container**

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

**Board Layout - Decoupling Circuit and Ground Planes**

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

**Board Layout - Hole Pattern**

The Agilent transceiver complies with the circuit board “Common Transceiver Footprint” hole pattern defined in the original multisource announcement which defined the 1 x 9 package style. This drawing is reproduced in Figure 8 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

**Board Layout - Mechanical**

For applications providing a choice of either a duplex SC or a duplex ST connector interface, while utilizing the same pinout on the printed circuit board, the ST port needs to protrude from the chassis panel a minimum of 9.53 mm for sufficient clearance to install the ST connector.

Please refer to Figure 8a for a mechanical layout detailing the recommended location of the duplex SC and duplex ST transceiver packages in relation to the chassis panel.

**DIMENSIONS ARE IN MILLIMETERS (INCHES)**

Figure 8. Recommended Board Layout Hole Pattern
Regulatory Compliance
These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Agilent sales representative.

Electrostatic Discharge (ESD)
There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Figure 8a. Recommended Common Mechanical Layout for SC and ST 1 x 9 Connector Transceivers.

NOTE 1: MINIMUM DISTANCE FROM FRONT OF CONNECTOR TO THE PANEL FACE.
Electromagnetic Interference (EMI)
Most equipment designs utilizing these high speed transceivers from Agilent will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

In all well-designed chassis, two 0.5" holes for ST connectors to protrude through will provide 4.6 dB more shielding than one 1.2" duplex SC rectangular cutout. Thus, in a well-designed chassis, the duplex ST 1 x 9 transceiver emissions will be identical to the duplex SC 1 x 9 transceiver emissions.

Immunity
Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing procedures and results on the 1 x 9 Transceiver family, please refer to Applications Note 1075, Testing and Measuring Electromagnetic Compatibility Performance of the AFBR-510X/520X Fiber Optic Transceivers.

Transceiver Reliability and Performance Qualification Data
The 1 x 9 transceivers have passed Agilent reliability and performance qualification testing and are undergoing ongoing quality monitoring. Details are available from your Agilent sales representative.

Accessory Duplex SC Connectored Cable Assemblies
Agilent recommends for optimal coupling the use of flexible-body duplex SC connected cable.

Accessory Duplex ST Connectored Cable Assemblies
Agilent recommends the use of Duplex Push-Pull connected cable for the most repeatable optical power coupling performance.
THE AFBR-5803Z OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE FOR RISE AND FALL TIME MEASUREMENTS.

Figure 10. Output Optical Pulse Envelope.

Figure 11. Relative Input Optical Power vs. Eye Sampling Time Position.

CONDITIONS:
1. $T_a = 25$ C
2. $V_{cc} = 5$ Vdc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 20 AND 21 APPLY.
Figure 12. Signal Detect Thresholds and Timing.

AS – MAX — MAXIMUM ACQUISITION TIME (SIGNAL).
AS – MAX IS THE MAXIMUM SIGNAL – DETECT ASSERTION TIME FOR THE STATION.
AS – MAX SHALL NOT EXCEED 100.0 µs. THE DEFAULT VALUE OF AS – MAX IS 100.0 µs.

ANS – MAX — MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS – MAX IS THE MAXIMUM SIGNAL – DETECT DEASSERTION TIME FOR THE STATION.
Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Reference</th>
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<td>Storage Temperature</td>
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<td>°C</td>
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<td></td>
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<td>sec.</td>
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<td>V</td>
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<tr>
<td>Data Input Voltage</td>
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<td>-0.5</td>
<td></td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
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<td>Differential Input Voltage</td>
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<td>1.4</td>
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<td>Note 1</td>
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<td>Output Current</td>
<td>$I_O$</td>
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<td>50</td>
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<td>mA</td>
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Recommended Operating Conditions

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<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Reference</th>
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<td>$T_A$</td>
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<td>°C</td>
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<td>AFBR-5803AZ/5803ATZ</td>
<td>$T_A$</td>
<td>-10</td>
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<td>+85</td>
<td>°C</td>
<td>Note B</td>
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<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
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<td>3.5</td>
<td>V</td>
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<tr>
<td></td>
<td>$V_{IL}$</td>
<td>4.75</td>
<td></td>
<td>5.25</td>
<td>V</td>
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<td>Data Input Voltage - Low</td>
<td>$V_I - V_{CC}$</td>
<td>-1.810</td>
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<td>-1.475</td>
<td>V</td>
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<td>Data Input Voltage - High</td>
<td>$V_I - V_{CC}$</td>
<td>-1.165</td>
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<td>-0.880</td>
<td>V</td>
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<tr>
<td>Data and Signal Detect Output Load</td>
<td>$R_L$</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
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Notes:
A. Ambient Operating Temperature corresponds to transceiver case temperature of 0°C minimum to +85 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.
B. Ambient Operating Temperature corresponds to transceiver case temperature of -10 °C minimum to +100 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.

Transmitter Electrical Characteristics
(AFBR-5803Z/5803TZ: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 3.135$ V to 3.5 V or 4.75 V to 5.25 V)
(AFBR-5803AZ/AFBR-5803ATZ: $T_A = -10^\circ C$ to $+85^\circ C$, $V_{CC} = 3.135$ V to 3.5 V or 4.75 V to 5.25 V)

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<td>Power Dissipation at $V_{CC} = 3.3$ V</td>
<td>$P_{Diss}$</td>
<td>0.45</td>
<td>0.6</td>
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<td>W</td>
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</tr>
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<td></td>
<td>$P_{Diss}$</td>
<td>0.76</td>
<td>0.97</td>
<td></td>
<td>W</td>
<td></td>
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<tr>
<td>Data Input Current - Low</td>
<td>$I_{IL}$</td>
<td>-360</td>
<td>-2</td>
<td></td>
<td>mA</td>
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<tr>
<td>Data Input Current - High</td>
<td>$I_{IH}$</td>
<td>18</td>
<td>350</td>
<td></td>
<td>μA</td>
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</table>
**Receiver Electrical Characteristics**
(AFBR-5803Z/5803TZ: $T_A = 0°C$ to $+70°C$, $V_{CC} = 3.135$ V to 3.5 V or 4.75 V to 5.25 V)
(AFBR-5803AZ/AFBR-5803ATZ: $T_A = -10°C$ to $+85°C$, $V_{CC} = 3.135$ V to 3.5 V or 4.75 V to 5.25 V)

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<th>Max.</th>
<th>Unit</th>
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<td>Supply Current</td>
<td>$I_{CC}$</td>
<td>-</td>
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<td>120</td>
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<td>Note 4</td>
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<tr>
<td>Power Dissipation at $V_{CC} = 3.3$ V</td>
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<td>0.25</td>
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<tr>
<td>Power Dissipation at $V_{CC} = 5.0$ V</td>
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<td>0.3</td>
<td>0.5</td>
<td>W</td>
<td>Note 5</td>
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<td>Data Output Voltage - Low</td>
<td>$V_{OL} - V_{CC}$</td>
<td>-1.83</td>
<td>-1.55</td>
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<td>Note 6</td>
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<td>Data Output Voltage - High</td>
<td>$V_{OH} - V_{CC}$</td>
<td>-1.085</td>
<td>-0.88</td>
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<td>Data Output Rise Time</td>
<td>$t_r$</td>
<td>0.35</td>
<td>2.2</td>
<td>ns</td>
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<td>Data Output Fall Time</td>
<td>$t_f$</td>
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<td>2.2</td>
<td>ns</td>
<td>Note 7</td>
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<td>Signal Detect Output Voltage - Low</td>
<td>$V_{OL} - V_{CC}$</td>
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<td>Note 6</td>
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<td>Signal Detect Output Voltage - High</td>
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<td>Signal Detect Output Rise Time</td>
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**Transmitter Optical Characteristics**
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<th>Max.</th>
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<td>Output Optical Power 62.5/125 µm, NA = 0.275 Fiber</td>
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<td>-14</td>
<td>dBm avg.</td>
<td>Note 11</td>
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<td>Output Optical Power 50/125 µm, NA = 0.20 Fiber</td>
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<td>dBm avg.</td>
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<td>Optical Extinction Ratio</td>
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<td>%</td>
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<td>Optical Extinction Ratio</td>
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<td>dB</td>
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<td>Output Optical Power at Logic “0” State</td>
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<td>dBm avg.</td>
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<td>Center Wavelength</td>
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<td>1308</td>
<td>1380</td>
<td>nm</td>
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<td>Spectral Width - FWHM</td>
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<td>Spectral Width - RMS</td>
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<td>Figure 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optical Rise Time</td>
<td>$t_r$</td>
<td>0.6</td>
<td>1.9</td>
<td>3.0</td>
<td>ns</td>
<td>Note 14, 15</td>
</tr>
<tr>
<td>Optical Fall Time</td>
<td>$t_f$</td>
<td>0.6</td>
<td>1.6</td>
<td>3.0</td>
<td>ns</td>
<td>Note 14, 15</td>
</tr>
<tr>
<td>Duty Cycle Distortion Contributed by the Transmitter</td>
<td>DCD</td>
<td>0.6</td>
<td></td>
<td>ns p-p</td>
<td>Note 16</td>
<td></td>
</tr>
<tr>
<td>Data Dependent Jitter Contributed by the Transmitter</td>
<td>DDJ</td>
<td>0.6</td>
<td></td>
<td>ns p-p</td>
<td>Note 17</td>
<td></td>
</tr>
<tr>
<td>Random Jitter Contributed by the Transmitter</td>
<td>RJ</td>
<td>0.69</td>
<td></td>
<td>ns p-p</td>
<td>Note 18</td>
<td></td>
</tr>
</tbody>
</table>
Notes:
1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to VCC - 2 V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to VCC - 2 V and an Input Optical Power level of -14 dBm average.
5. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6. This value is measured with respect to VCC with the output terminated into 50 Ω connected to VCC - 2 V.
7. The output rise and fall times are measured between 20% and 80% levels with the output connected to VCC - 2 V through 50 Ω.
8. Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold using an IDLE Line State, 125 Mb/s (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average. See Application Information - Transceiver Jitter Section for further information.
9. Data Dependent Jitter contributed by the receiver is specified with the FDDI DDJ test pattern described in the FDDI PMD Annex A.5. The input optical power level is -20 dBm average. See Application Information - Transceiver Jitter Section for further information.
10. Random Jitter contributed by the receiver is specified with an IDLE Line State, 125 Mb/s (62.5 MHz square-wave), input signal. The input optical power level is at maximum "PIN Min. (W)". The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.
11. The transmitter provides compliance with the need for Transmit_Disable commands from the FDDI SMT layer by providing an Output Optical Power level of < -45 dBm average in response to a logic "0" input. This specification applies to either 62.5/125 µm or 50/125 µm fiber cables.
14. This parameter complies with the FDDI PMD requirements for the trade-offs between center wavelength, spectral width, and rise/fall times shown in Figure 9.

15. This parameter complies with the optical pulse envelope from the FDDI PMD shown in Figure 10. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.

16. Duty Cycle Distortion contributed by the transmitter is measured at a 50% threshold using an IDLE Line State, 125 Mb/s (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.

17. Data Dependent Jitter contributed by the transmitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.

18. Random Jitter contributed by the transmitter is specified with an IDLE Line State, 125 Mb/s (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.

19. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5 x 10^-10.

• At the Beginning of Life (BOL)
• Over the specified operating temperature and voltage ranges
• Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
• Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM. _Data indication input (PHY input) per the example in FDDI PMD Annex E.

This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active input jitter condition requires exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the cumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.8 ns - 0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns.

This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst case input jitter conditions to the Agilent receiver.
  • Transmitter operating with an IDLE Line State pattern, 125 Mb/s (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

20. All conditions of Note 19 apply except that the measurement is made at the center of the symbol with no window time-width.

21. This value is measured during the transition from low to high levels of input optical power.

22. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, -45 dBm, into the range between greater than P_A and -14 dBm. The BER of the receiver output will be 10^-2 or better during the time, LS_Max (15 µs) after Signal Detect has been asserted. See Figure 12 for more information.

23. This value is measured during the transition from high to low levels of input optical power. The maximum value will occur when the input optical power is either -45 dBm average or when the input optical power yields a BER of 10^-2 or larger, whichever power is higher.

24. Signal detect output shall be de-asserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of: -31 dBm or P_A + 4 dB (P_P is the power level at which signal detect was de-asserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^-2 or better for a period of 12 µs or until signal detect is de-asserted. The input data stream is the Quiet Line State. Also, signal detect will be de-asserted within a maximum of 350 µs after the BER of the receiver output degrades above 10^-2 for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 12 for more information.
Ordering Information
The AFBR-5803Z/5803TZ/5803AZ/5803ATZ 1300 nm products are available for production orders through the Agilent Component Field Sales Offices and Authorized Distributors worldwide.

0 °C to +70 °C
AFBR-5803Z/5803TZ

-10 °C to +85 °C
AFBR-5803AZ/5803ATZ

Note:
The “T” in the product numbers indicates a transceiver with a duplex ST connector receptacle.
Product numbers without a “T” indicate transceivers with a duplex SC connector receptacle.