AN-8027
FAN480X PFC+PWM Combination Controller Application
FAN4800A / FAN4800C / FAN4801 / FAN4802 / FAN4802L

Introduction

This application note describes step-by-step design considerations for a power supply using the FAN480X controller. The FAN480X combines a PFC controller and a PWM controller. The PFC controller employs average current mode control for Continuous Conduction Mode (CCM) boost converter in the front end. The PWM controller can be used in either current mode or voltage mode for the downstream converter. In voltage mode, feed-forward from the PFC output bus can be used to improve the line transient response of PWM stage. In either mode, the PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This proprietary leading/trailing-edge modulation technique can significantly reduce the ripple current of the PFC output capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). In addition to power factor correction, a number of protection features have been built in to the FAN480X. These include programmable soft-start, PFC over-voltage protection, pulse-by-pulse current limiting, brownout protection, and under-voltage lockout.

FAN4801/2/2L feature programmable two-level PFC output to improve efficiency at light-load and low-line conditions.

FAN480X is pin-to-pin compatible with FAN4800 and ML4800, only requiring adjustment of some peripheral components. The FAN480X series comparison is summarized in the Appendix A.

Figure 1. Typical Application Circuit of FAN480X
Functional Description

Gain Modulator

The gain modulator is the key block for PFC stage because it provides the reference to the current control error amplifier for the input current shaping, as shown in Figure 2. The output current of gain modulator is a function of \( V_{EA} \), \( I_{AC} \), and \( V_{RMS} \). The gain of the gain modulator is given in the datasheet as a ratio between \( I_{M0} \) and \( I_{AC} \) with a given \( V_{RMS} \) when \( V_{EA} \) is saturated to HIGH. The gain is inversely proportional to \( V_{RMS}^2 \), as shown in Figure 3, to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage such that the input power of PFC converter is not changed with line voltage.

\[
IG(0.7) = I_{M0}(0.7) \frac{V_{V}}{V_{EA}}\frac{V_{EA}}{V_{EA} - 0.7}
\]

Figure 2. Gain Modulator Block

However, once PFC stops switching operation, the junction capacitance of bridge diode is not discharged and \( V_{IN} \) of Figure 2 is clamped at the peak of the line voltage. Then, the voltage of VRMS pin is given by:

\[
V_{RMS} = \frac{\sqrt{2} R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \cdot \frac{2}{\pi}
\]

Therefore, the voltage divider for VRMS should be designed considering the brownout protection trip point and minimum operation line voltage.

Figure 4. \( V_{RMS} \) According to the PFC Operation

To sense the RMS value of the line voltage, an averaging circuit with two poles is typically employed, as shown in Figure 2. The voltage of VRMS pin in normal PFC operation is given as:

\[
V_{RMS} = V_{LINE} \sqrt{\frac{2}{\pi}} \cdot \frac{2}{\pi}
\]

where \( V_{LINE} \) is RMS value of line voltage.

Current and Voltage Control of Boost Stage

As shown in Figure 5, the FAN480X employs two control loops for power factor correction: a current control loop and a voltage control loop. The current control loop shapes inductor current, as shown in Figure 6, based on the reference signal obtained at the IAC pin as:

\[
I_{L} \cdot R_{CS1} = I_{MO} \cdot R_{W} = I_{AC} \cdot G \cdot R_{M}
\]

where \( V_{LINE} \) is the line voltage that trips brownout protection, \( G_{MAX} \) is the maximum modulator gain when \( V_{RMS} \) is 1.08V (which can be found in the datasheet), and 159µA is the maximum output current of the gain modulator.
The voltage control loop regulates PFC output voltage using internal error amplifier such that the FBPFC voltage is same as internal reference of 2.5V.

**Brownout Protection**

FAN480X has a built-in internal brownout protection comparator monitoring the voltage of the VRMS pin. Once the VRMS pin voltage is lower than 1.05V (0.9V for FAN4802L), the PFC stage is shutdown to protect the system from over current. The FAN480X starts up the boost stage once the VRMS voltage increases above 1.9V (1.65V for FAN4802L).

**Two-Level PFC Output**

To improve system efficiency at low AC line voltage and light load condition, FAN480X provides two-level PFC output voltage. As shown in Figure 7, FAN480X monitors V_{EA} and V_{RMS} voltages to adjust the PFC output voltage. When V_{EA} and V_{RMS} are lower than the thresholds, an internal current source of 20 µA is enabled that flows through R_{FB2}, increasing the voltage of the FBPFC pin. This causes the PFC output voltage to reduce when 20 µA is enabled, calculated as:

\[ V_{OPFC2} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times (2.5 \times 20 \mu A \times R_{FB1}) \]  \hspace{1cm} (5)

It is typical to set the second boost output voltage as 340V~300V.

The internal oscillator frequency of FAN480X is determined by the timing resistor and capacitor on RT/CT pin. The frequency of the internal oscillator is given by:

\[ f_{OSC} = \frac{1}{0.56 \times R_{CT} \times C_{T} + 360C_{T}} \]  \hspace{1cm} (6)

Because the PWM stage of FAN480X generally uses a forward converter, it is required to limit the maximum duty cycle at 50%. To have a small tolerance of the maximum duty cycle, a frequency divider with toggle flip-flops is used, as illustrated in Figure 8. The operation frequency of PFC and PWM stage is one quarter (1/4) of the oscillator frequency. (For FAN4800C and FAN4802/2L, the operation frequencies for PFC and PWM stages are one quarter (1/4) and one half (1/2) of the oscillator frequency, respectively).

The dead time for the PFC gate drive signal is determined by the equation:

\[ I_{DEAD} = 360C_{T} \]  \hspace{1cm} (7)

The dead time should be smaller than 2% of switching period to minimize line current distortion around line zero crossing.
PWM Stage

The PWM stage is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage and is thereby representative of the current flowing in the converter’s output stage. ILIMIT, which provides cycle-by-cycle current limiting, is typically connected to RAMP in such applications.

For voltage-mode operation, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which FBPWM voltage is compared. Under these conditions, the use of voltage feed-forward from the PFC bus can be used for better line transient response.

No voltage error amplifier is included in the PWM stage, as this function is generally performed by a programmable shunt regulator, such as KA431, in the secondary-side. To facilitate the design of opto-coupler feedback circuitry, an offset voltage is built into the inverting input of PWM comparator that allows FBPWM to command a zero percent duty cycle when its pin voltage is below 1.5V.

PWM Current Limit

The ILIMIT pin is a direct input to the cycle-by-cycle current limiter for the PWM section. If the input voltage at this pin exceeds 1V, the output of the PWM is disabled until the start of the next PWM clock cycle.

VIN OK Comparator

The VIN OK comparator monitors the output of the PFC stage and inhibits the PWM stage if this voltage is less than 2.4V (96% of its nominal value). Once this voltage goes above 2.4V, the PWM stage begins to soft-start.

PWM Soft-Start (SS)

PWM startup is controlled by the soft-start capacitor. A 10μA current source supplies the charging current for the soft-start capacitor. Startup of the PWM is prohibited until the soft-start capacitor voltage reaches 1.5V.
Design Considerations

In this section, a design procedure is presented using the schematic in Figure 11 as reference. A 300W PC power supply application with universal input range is selected as a design example. The design specifications are summarized in Table 1. The two-switch forward converter is used for DC/DC converter stage.

### Design Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Voltage of Output 1</td>
<td>$V_{OUT1} = 5V$</td>
</tr>
<tr>
<td>Rated Current of Output 1</td>
<td>$I_{OUT1} = 9A$</td>
</tr>
<tr>
<td>Rated Voltage of Output 2</td>
<td>$V_{OUT2} = 12V$</td>
</tr>
<tr>
<td>Rated Current of Output 2</td>
<td>$I_{OUT2} = 16.5A$</td>
</tr>
<tr>
<td>Rated Voltage of Output 3</td>
<td>$V_{OUT3} = -12V$</td>
</tr>
<tr>
<td>Rated Current of Output 3</td>
<td>$I_{OUT3} = 0.8A$</td>
</tr>
<tr>
<td>Rated Voltage of Output 4</td>
<td>$V_{OUT4} = 3.3V$</td>
</tr>
<tr>
<td>Rated Current of Output 4</td>
<td>$I_{OUT4} = 13.5A$</td>
</tr>
<tr>
<td>Rated Output Power</td>
<td>$P_O = 300W$</td>
</tr>
<tr>
<td>Line Voltage Range</td>
<td>85~264V$_{AC}$</td>
</tr>
<tr>
<td>Line Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Brownout Protection Line Voltage</td>
<td>72V$_{AC}$</td>
</tr>
<tr>
<td>Overall Stage Efficiency</td>
<td>$\eta = 0.82$</td>
</tr>
<tr>
<td>PWM Stage Efficiency</td>
<td>$\eta_{PWM} = 0.86$</td>
</tr>
<tr>
<td>Hold-up Time</td>
<td>$t_{HLD} = 20ms$</td>
</tr>
<tr>
<td>Minimum PFC Output Voltage</td>
<td>310V</td>
</tr>
<tr>
<td>Nominal PFC output voltage</td>
<td>$V_{O,PFC} = 387V$</td>
</tr>
<tr>
<td>PFC Inductor Ripple Current</td>
<td>$dI = 40%$</td>
</tr>
<tr>
<td>AC Input Voltage Frequency</td>
<td>$f_{line} = 50 ~ 60$Hz</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>$\alpha = 4%$</td>
</tr>
<tr>
<td>Magnetic Flux Density</td>
<td>$\Delta B = 0.27T$</td>
</tr>
<tr>
<td>Current Density</td>
<td>$D_{cma} = 400C-m/A$</td>
</tr>
<tr>
<td>PWM Maximum Duty Cycle</td>
<td>$D_{max} = 0.35$</td>
</tr>
<tr>
<td>5V Output Current Ripple</td>
<td>$I_{OUT1} = 44%$</td>
</tr>
<tr>
<td>12V Output Current Ripple</td>
<td>$I_{OUT2} = 10%$</td>
</tr>
</tbody>
</table>

**Figure 11. Reference Circuit for Design Example**
[STEP-1] Define System Specifications

Since the overall system is comprised of two stages (PFC and DC/DC), as shown in Figure 12, the input power and output power of the boost stage are given as:

\[ P_{IN} = \frac{P_{OUT}}{\eta} \]  \hspace{1cm} (8)

\[ P_{BOUT} = \frac{P_{OUT}}{\eta_{PWM}} \]  \hspace{1cm} (9)

where \( \eta \) is the overall efficiency and \( \eta_{PWM} \) is the forward converter efficiency.

The nominal output current of boost PFC stage is given as:

\[ I_{BOUT} = \frac{P_{BOUT}}{V_{BOUT} \eta_{PWM}} \]  \hspace{1cm} (10)

(Design Example) Since the switching frequency is 65kHz, \( C_T \) is selected as 1nF. Then the maximum duty cycle of PFC gate drive signal is obtained as:

\[ D_{\text{MAX,PFC}} = 1 - 360 \cdot C_T \cdot f_{SW} = 0.98 \]

The timing resistor is determined as:

\[ R_T = \frac{1}{4} \cdot \frac{1}{0.56 f_{SW} C_T} = 6.9k\Omega \]

[STEP-2] Frequency Setting

The switching frequency is determined by the timing resistor and capacitor (\( R_T \) and \( C_T \)) as:

\[ f_{SW} \approx \frac{1}{4} \cdot \frac{1}{0.56 \cdot R_T \cdot C_T} \]  \hspace{1cm} (11)

It is typical to use a 470pF~1nF capacitor for 50~75kHz switching frequency operation since the timing capacitor value determines the maximum duty cycle of PFC gate drive signal as:

\[ D_{\text{MAX,PFC}} = 1 - \frac{T_{OFF,MIN}}{T_{SW}} = 1 - 360 \cdot C_T \cdot f_{SW} \]  \hspace{1cm} (12)

(Design Example) Since the switching frequency is 65kHz, \( C_T \) is selected as 1nF. Then the maximum duty cycle of PFC gate drive signal is obtained as:

\[ D_{\text{MAX,PFC}} = 1 - 360 \cdot C_T \cdot f_{SW} = 0.98 \]

The timing resistor is determined as:

\[ R_T = \frac{1}{4} \cdot \frac{1}{0.56 f_{SW} C_T} = 6.9k\Omega \]

[STEP-3] Line Sensing Circuit Design

FAN480X senses the RMS value and instantaneous value of line voltage using the VRMS and IAC pins, respectively, as shown in Figure 13. The RMS value of the line voltage is obtained by an averaging circuit using low pass filter with two poles. Meanwhile, the instantaneous line voltage information is obtained by sensing the current flowing into IAC pin through \( R_{IAC} \).

RMS sensing circuit should be designed considering the nominal operation range of line voltage and brownout protection trip point as:

\[ V_{\text{RMS-UVL}} = V_{\text{LINE,BO}} \cdot \frac{\sqrt{2} R_{\text{RMS3}}}{R_{\text{RMS1}} + R_{\text{RMS2}} + R_{\text{RMS3}}} = \frac{2}{\pi} \]  \hspace{1cm} (13)

\[ V_{\text{RMS-UVH}} < V_{\text{LINE,MIN}} \cdot \frac{\sqrt{2} R_{\text{RMS3}}}{R_{\text{RMS1}} + R_{\text{RMS2}} + R_{\text{RMS3}}} \]  \hspace{1cm} (14)

where \( V_{\text{RMS-UVL}} \) and \( V_{\text{RMS-UVH}} \) are the brown OUT/IN thresholds of \( V_{\text{RMS}} \).

It is typical to set \( R_{\text{RMS2}} \) as 10% of \( R_{\text{RMS1}} \). The poles of the low pass filter are given as:

\[ f_{p1} = \frac{1}{2\pi \cdot R_{\text{RMS1}} \cdot C_{\text{RMS1}}} \]  \hspace{1cm} (15)

\[ f_{p2} = \frac{1}{2\pi \cdot R_{\text{RMS2}} \cdot C_{\text{RMS2}}} \]  \hspace{1cm} (16)
To properly attenuate the twice line frequency ripple in VRMS, it is typical to set the poles around 10–20Hz. The resistor R_IAC should be large enough to prevent saturation of the gain modulator as:

\[ \frac{\sqrt{2}V_{\text{LINE,BO}}}{R_{\text{IAC}}} G_{\text{MAX}} < 159 \mu A \]  \hspace{1cm} (17)

where V_{LINE,BO} is the brownout protection line voltage, G_{MAX} is the maximum modulator gain when VRMS is 1.08V (which can be found in the datasheet), and 159\mu A is the maximum output current of the gain modulator.

**[Design Example]** The brownout protection threshold is 1.05V (V_{RMS,UVL}) and 1.9V (V_{RMS,UVH}), respectively. Then, the scaling down factor of the voltage divider is:

\[ \frac{1.05}{\sqrt{2}} \cdot \frac{V_{\text{LINE,BO}}}{2\sqrt{2}} = 0.0162 \]

Then the startup of the PFC stage at the minimum line voltage is checked as:

\[ \frac{V_{\text{LINE,MIN}} \cdot \sqrt{2} R_{\text{RMS1}}}{R_{\text{RMS1}} + R_{\text{RMS2}} + R_{\text{RMS3}}} = 85 \cdot \sqrt{2} \cdot 0.0162 = 1.95 > 1.9V \]

The resistors of the voltage divider network are selected as R_{RMS1}=2M\Omega, R_{RMS2}=200k\Omega, and R_{RMS3}=36k\Omega.

To place the poles of the low pass filter at 15Hz and 22Hz, the capacitors are obtained as:

\[ C_{\text{RMS1}} = \frac{1}{2\pi \cdot f_{p1} \cdot R_{\text{RMS2}}} = \frac{1}{2\pi \cdot 15 \cdot 200 \times 10^3} = 53nF \]
\[ C_{\text{RMS2}} = \frac{1}{2\pi \cdot f_{p2} \cdot R_{\text{RMS3}}} = \frac{1}{2\pi \cdot 22 \cdot 36 \times 10^3} = 200nF \]

The condition for Resistor R_{IAC} is:

\[ R_{\text{IAC}} > \frac{\sqrt{2} V_{\text{LINE,BO}}}{159 \times 10^3} G_{\text{MAX}} = \frac{\sqrt{2} \cdot 72.9}{159 \times 10^3} = 5.8M\Omega \]

Therefore, 6M\Omega resistor is selected for R_{IAC}.

**[STEP-4] PFC Inductor Design**

The duty cycle of boost switch at the peak of line voltage is given as:

\[ D_{LP} = \frac{V_{\text{BOUT}} - \sqrt{2} V_{\text{LINE}}}{V_{\text{BOUT}}} \]  \hspace{1cm} (18)

Then, the maximum current ripple of the boost inductor at the peak of line voltage for low line is given as:

\[ \Delta I_l = \frac{\sqrt{2} V_{\text{LINE,MIN}}}{V_{\text{BOOST}}} \cdot \frac{V_{\text{BOUT}} - \sqrt{2} V_{\text{LINE}}}{V_{\text{BOUT}}} \cdot \frac{1}{f_{SW}} \]  \hspace{1cm} (19)

The average of boost inductor current over one switching cycle at the peak of the line voltage for low line is given as:

\[ I_{L,AVG} = \frac{\sqrt{2} P_{\text{OUT}}}{V_{\text{LINE,MIN}} \cdot \eta} \]  \hspace{1cm} (20)

Therefore, with a given current ripple factor (K_{RB}=\Delta I/I_{L,AVG}), the boost inductor value is obtained as:

\[ L_{\text{BOOST}} = \frac{V_{\text{LINE,MIN}} \cdot \eta}{K_{RB} \cdot P_{\text{OUT}}} \cdot \frac{V_{\text{BOUT}} - \sqrt{2} V_{\text{LINE}}}{V_{\text{BOUT}}} \cdot \frac{1}{f_{SW}} \]  \hspace{1cm} (21)

The maximum current of boost inductor is given as:

\[ I_{L,PK} = I_{L,AVG} \cdot (1 + \frac{K_{RB}}{2}) = \frac{\sqrt{2} P_{\text{OUT}}}{V_{\text{LINE,MIN}} \cdot \eta} \cdot (1 + \frac{K_{RB}}{2}) \]  \hspace{1cm} (22)

**[STEP-5] PFC Output Capacitor Selection**

The output voltage ripple should be considered when selecting the PFC output capacitor. Figure 14 shows the twice line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

\[ \frac{I_{\text{BOUNTS}}}{2\pi \cdot f_{\text{LINE}} \cdot V_{\text{BOUNTS,ripple}}} \]  \hspace{1cm} (23)

where I_{BOUNTS} is nominal output current of boost PFC stage and V_{BOUNTS,ripple} is the peak-to-peak output voltage ripple specification.

The hold-up time also should be considered when determining the output capacitor as:

\[ C_{\text{BOUNTS}} > \frac{P_{\text{BOUNTS}} \cdot t_{\text{HOLD}}}{V_{\text{BOUNTS}} - V_{\text{BOUNTS,MIN}}} \]  \hspace{1cm} (24)

where P_{BOUNTS} is nominal output power of boost PFC stage, t_{HOLD} is the required holdup time, and V_{BOUNTS,MIN} is the allowable minimum PFC output voltage during hold-up time.
(Design Example) With the ripple specification of 12Vpp, the capacitor should be:

\[ C_{\text{BOUT}} > \frac{I_{\text{BOUT}}}{2\pi \cdot f_{\text{LINE}} \cdot V_{\text{BOUT, RIPPLE}}} = \frac{0.9}{2\pi \cdot 50 \cdot 12} = 239 \mu F \]

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 310V, the capacitor should be:

\[ C_{\text{BOUT}} > \frac{P_{\text{BOUT}} \cdot t_{\text{HOLD}}}{V_{\text{OUT}}^2 - V_{\text{OUT, MIN}}^2} = \frac{2 \cdot 349 \cdot 20 \times 10^{-3}}{387^2 - 310^2} = 260 \mu F \]

Thus, 270\mu F capacitor is selected for the PFC output capacitor.

[STEP-6] PFC Output Sensing Circuit

To improve system efficiency at low line and light load condition, FAN480X provides two-level PFC output voltage. As shown in Figure 15, FAN480X monitors \( V_{\text{EA}} \) and \( V_{\text{RMS}} \) voltages to adjust the PFC output voltage.

The PFC output voltage when 20\( \mu \)A is enabled is given as:

\[ V_{\text{BOUT}2} = V_{\text{BOUT}} \times \left( 1 - \frac{20 \mu A \times R_{FB2}}{2.5} \right) \quad (25) \]

It is typical second boost output voltage as 340V~300V.

(Design Example) Assuming the second level of PFC output voltage is 347V:

\[ R_{FB2} = \left( 1 - \frac{V_{\text{BOUT2}}}{V_{\text{BOUT}}} \right) \cdot \frac{2.5}{20 \times 10^{-6}} \]

\[ = \left( 1 - \frac{347}{387} \right) \cdot \frac{2.5}{20 \times 10^{-6}} = 12.9k\Omega \]

13k\( \Omega \) is selected for \( R_{FB2} \).

\[ R_{FB1} = (V_{\text{BOUT}} - 1) \cdot R_{FB2} \]

\[ = \left( \frac{387}{2.5} - 1 \right) \cdot 13 \times 10^3 = 1999k\Omega \]

2M\( \Omega \) is selected for \( R_{FB1} \).

[STEP-7] PFC Current-Sensing Circuit Design

Figure 16 shows the PFC compensation circuits. The first step in compensation network design is to select the current-sensing resistor of PFC converter considering the control window of voltage loop. Since line feed-forward is used in FAN480X, the output power is proportional to the voltage control error amplifier voltage as:

\[ P_{\text{BOUT}}(V_{\text{EA}}) = P_{\text{BOUT}}^{\text{MAX}} \cdot \frac{V_{\text{EA}}}{V_{\text{EA}}^{\text{SAT}}} - 0.6 \quad (27) \]

where \( V_{\text{EA}}^{\text{SAT}} \) is 5.6V and the maximum power limit of PFC is:

\[ P_{\text{BOUT}}^{\text{MAX}} = \frac{V_{\text{LINE,BG}}^2 \cdot G^{\text{MAX}} \cdot R_{\text{IN}}}{R_{\text{CSI}}} \quad (28) \]
It is typical to set the maximum power limit of PFC stage around 1.2~1.5 of its nominal power such that the V_{EA} is around 4~4.5V at nominal output power. By adjusting the current-sensing resistor for PFC stage, the maximum power limit of PFC stage can be programmed.

To filter out the current ripple of switching frequency, an RC filter is typically used for ISENSE pin. R_{LF1} should not be larger than 100Ω and the cut-off frequency of filter should be 1/2~1/6 of the switching frequency.

Diodes D1 and D2 are required to prevent over-voltage on ISENSE pin due to the inrush current that might damage the IC. A fast recovery diode or ultra fast recovery diode is recommended.

![Gain Modulation Block](figure)

**Figure 16. Gain Modulation Block**

(Design Example) Setting the maximum power limit of PFC stage as 450W, the current sensing resistor is obtained as:

\[
R_{CS1} = \frac{V_{LINE,BO}^2 \cdot G_{MAX}}{P_{OUT,MAX}} = \frac{72^2 \cdot 9.5-5.7 \cdot 10^3}{6 \cdot 10^3 \cdot 450} = 0.098Ω
\]

Thus, 0.1Ω resistor is selected.

[STEP-8] PFC Current Loop Design

The transfer function from duty cycle to the inductor current of boost power stage is given as:

\[
\frac{d\dot{i}_L}{dt} = \frac{V_{BOUT}}{sT_{BOOST}}
\]  

(29)

The transfer function from the output of the current control error amplifier to the inductor current-sensing voltage is obtained as:

\[
\frac{\hat{v}_{CS}}{\hat{v}_{IEA}} = \frac{R_{CS1} \cdot V_{BOUT}}{\hat{V}_{RAMP} \cdot sL_{BOOST}}
\]

(30)

where \(V_{RAMP}\) is the peak to peak voltage of ramp signal for current control PWM comparator, which is 2.55V.

The transfer function of the compensation circuit is given as:

\[
\frac{\hat{v}_{IEA}}{\hat{V}_{CS1}} = \frac{\frac{1 + \frac{s}{2\pi f_p}}{s} + \frac{1 + \frac{s}{2\pi f_p}}{2\pi f_p}}{2\pi f_p \cdot R_{IC} \cdot C_{IC1} + 1}
\]

(31)

where:

\[
f_p = \frac{G_{MI}}{2\pi \cdot C_{IC1}}, \quad f_C = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC1}} \quad \text{and}
\]

\[
f_{IC} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC2}}
\]

(32)

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (\(f_{IC}\)) around 1/10~1/6 of the switching frequency. Then calculate the gain of the transfer function of Equation (30) at crossover frequency as:

\[
\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}} \bigg|_{f_{IC}} = \frac{R_{CS1} \cdot V_{BOUT}}{\hat{V}_{RAMP} \cdot 2\pi f_p \cdot L_{BOOST}}
\]

(33)

(b) Calculate \(R_{IC}\) that makes the closed loop gain unity at crossover frequency:

\[
R_{IC} = \left( \frac{1}{G_{MI}} \cdot \frac{\hat{V}_{CS1}}{\hat{v}_{IEA}} \bigg|_{f_{IC}} \right)^{-1}
\]

(34)

(c) Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency is 0dB, as shown in Figure 17; it is necessary to place the zero of the compensation network (\(f_{IZ}\)) around 1/3 of the crossover frequency so that more than 45° phase margin is obtained. Then the capacitor \(C_{IC1}\) is determined as:

\[
C_{IC1} = \frac{1}{R_{IC} \cdot 2\pi f_p / 3}
\]

(35)

(d) Place compensator high-frequency pole (\(f_{CP}\)) at least a decade higher than \(f_{IC}\) to ensure that it does not interfere with the phase margin of the current loop at its crossover frequency.

\[
C_{IC2} = \frac{1}{2\pi \cdot f_p \cdot R_{IC}}
\]

(36)
Figure 17. Current Loop Compensation

(Design Example) Setting the crossover frequency as 7kHz:

\[ \frac{v_{CS}}{v_{IEA}}_{|s_f=f_C} = \frac{R_{CS} \cdot V_{BOUT}}{V_{RAMP} \cdot 2\pi f_{IEA} \cdot I_{BOOST}} = 0.137 \approx 0.66 \]

\[ R_{IE} = \frac{1}{G_{MV} \cdot \frac{v_{CS}}{v_{IEA}}_{|s_f=f_C}} = \frac{1}{88 \times 10^6 \cdot 0.66} = 17k\Omega \]

\[ C_{IC1} = \frac{1}{R_{IE} \cdot 2\pi f_{IE} / 3} = \frac{1}{17 \times 10^3 \cdot 2\pi \cdot 7 \times 10^3 / 3} = 4nF \]

Setting the pole of the compensator at 70kHz,

\[ C_{IC2} = \frac{1}{2\pi f_{IP} R_{IE}} = \frac{1}{2\pi \cdot 70 \times 10^3 \cdot 17 \times 10^3} = 0.13nF \]

Figure 18. Voltage Loop Compensation

The transfer function of the compensation network is obtained as:

\[ \frac{v_{COMP}}{v_{OUT}} = \frac{2\pi f_{vz}}{s + 1 + \frac{s}{2\pi f_{vz}}} \]

where:

\[ f_{vz} = \frac{2.5}{V_{BOUT} \cdot C_{VC1}} \quad f_{IP} = 2\pi f_{vz} \cdot C_{VC1} \]

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency \( f_{VC} \) around 1/10~1/5 of the line frequency. Since the control-to-output transfer function of power stage has a -20dB/dec slope and -90° phase at the crossover frequency, as shown in Figure 18 as 0dB; it is necessary to place the zero of the compensation network \( f_{VZ} \) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitor \( C_{VC1} \) is determined as:

\[ C_{VC1} = \frac{G_{MV} \cdot J_{BOUT} \cdot K_{MAX}}{5 \cdot C_{BOUT} \cdot (2\pi f_{VC})^2} \cdot \frac{2.5}{V_{BOUT}} \]

(b) Place compensator high-frequency pole \( f_{VP} \) at least a decade higher than \( f_{C} \) to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor \( C_{VC2} \) is determined as:

\[ C_{VC2} = \frac{1}{2\pi f_{IP} R_{VC}} \]
**AN-8027**

© 2009 Fairchild Semiconductor Corporation  www.fairchildsemi.com

**Rev. 1.0.0  •  8/26/09**

**[Design Example]** Setting the crossover frequency as 22Hz:

\[
C_{\text{fC1}} = \frac{G_{\text{Mv}} \cdot I_{\text{BOUT}} \cdot K_{\text{MAX}} \cdot 2.5}{5 \cdot C_{\text{BOUT}} \cdot (2\pi f_{\text{fC1}})^2} \cdot \frac{2.5}{V_{\text{BOUT}}} = \frac{70 \times 10^{-6} \cdot 0.9 \cdot 1.27 \cdot 2.5}{5 \cdot 270 \times 10^{-6} \cdot (2\pi \cdot 22)^2} = 20 \text{nF}
\]

\[
R_{\text{fC}} = \frac{1}{2\pi \cdot f_{\text{fC}} \cdot C_{\text{fC1}}} = \frac{1}{2\pi \cdot 22 \cdot 10^{-9}} = 362 \text{k}\Omega
\]

Setting the pole of the compensator at 120Hz:

\[
C_{\text{fC2}} = \frac{1}{2\pi \cdot f_{\text{fC}} \cdot R_{\text{fC}}} = \frac{1}{2\pi \cdot 120 \cdot 362 \times 10^3} = 3.7 \text{nF}
\]

**[STEP-10] Transformer Design for PWM Stage**

Figure 19 shows the typical secondary-side circuit of a forward converter for multi-output of PC power application.

A common technique for winding multiple outputs with the same polarity sharing a common ground is to stack the secondary windings instead of winding each output winding separately. This approach improves the load regulation of the stacked outputs. The winding \( N_{S1} \) in Figure 19 must be sized to accommodate its output current, plus the current of the output (+12V) stacked on top of it. To get tight regulation of 3.3V output, magnetic amplifier (MAG-AMP) is used. The saturable core of MAG-AMP prevents the diode \( D_{\text{REC}} \) from fully conducting by introducing high impedance until it is saturated. This allows the effective duty cycle of \( V_{\text{REC}} \) to be controlled to be regulated the output voltage.

The golden ratio between the secondary-side windings for the best regulation of 3.3V, 5V, and 12V is known as 2:3:7.

**Design Example** The minimum PFC output voltage is 310V and the maximum duty cycle of PWM controller is 50%. By adding 5% margin to the maximum duty cycle, \( D_{\text{MAX}}=0.45 \) is used for transformer design. Assuming ERL35 \((Ae=107 \text{mm}^2)\) core is used and \( \Delta B=0.28 \), the minimum turns for the transformer primary-side is obtained as:

\[
N_p^\text{MIN} = \frac{V_{\text{BOUT}} \cdot D_{\text{MAX}}}{A_e \cdot f_{SW} \cdot \Delta B} = \frac{310 \cdot 0.45}{107 \times 10^{-6} \cdot 0.65 \times 10^{-3} \cdot 0.28} = 72
\]

The turns ratio for 5V output is obtained as:

\[
n = \frac{N_p}{N_{S1}} = \frac{V_{\text{BOUT}} \cdot D_{\text{MAX}}}{V_{O1} + V_f} = \frac{310 \cdot 0.45}{5 + 0.45} = 25.6
\]

The number of turns for the primary-side winding is determined as:

\[
N_p = n \cdot N_{S1} = 2 \times 25.6 = 51.2 < N_p^\text{MIN}
\]

\[
N_p = n \cdot N_{S1} = 3 \times 25.6 = 76.8 > N_p^\text{MIN} \quad : \quad N_{S1} = 3
\]

Then, the turns ratio for 12V output is obtained as:

\[
N_{S2} = \frac{V_{O2} + V_f}{V_{O1} + V_f} \cdot N_{S1} = \frac{12 + 0.7}{5 + 0.45} \cdot 3 = 6.99 \pm 7
\]

Therefore, the number of turns for each winding is obtained as:

\( N_p=78, N_{S1}=3, N_{S2}=7 (3+4 \text{ stack}) \) and \( N_{S3}=7 \).
[STEP-11] Coupled Inductor Design for the PWM Stage

When the forward converter has more than one output, as shown in Figure 20, coupled inductors are usually employed to improve the cross regulation and to reduce the ripple. They are implemented by winding their separate coils on a single, common core. The turns ratio should be the same as the transformer turns ratio of the two outputs as:

\[
\frac{N_{S2}}{N_{S1}} = \frac{N_{L2}}{N_{L1}}
\]

(47)

One way to understand the operation of coupled inductor is to normalize the outputs to one output. Figure 21 shows how to normalize the second output (V\(_{O2}\)) to the first output (V\(_{O1}\)). The transformer and inductor turns are divided by N\(_{S2}/N_{S1}\), the voltage and current are adjusted by N\(_{S2}/N_{S1}\). It is assumed that the leakage inductances of the coupled inductor are much smaller than the magnetizing inductance and evenly distributed for each winding.

The inductor value of the first output can be obtained by:

\[
L_1 = \frac{V_{O1}(V_{O1}+V_{F1})}{f_{SW}(P_{O1}+P_{O2})} \frac{\Delta I_{SUM}}{I_{SUM}} (1 - D_{MIN})
\]

(48)

where:

\[
D_{MIN} = D_{MAX} \frac{V_{ROUT}_{MIN}}{V_{ROUT}}
\]

(49)

Then, the ripple current for each output is given as:

\[
\frac{\Delta I_{O1}}{I_{O1}} = \frac{\Delta I_{SUM}}{2} \frac{1}{I_{O1}}
\]

(50)

\[
\frac{\Delta I_{O2}}{I_{O2}} = \frac{\Delta I_{SUM}}{2} \frac{N_{S1}}{N_{S2}} \frac{1}{I_{O2}}
\]

(51)

(Design Example) The minimum duty cycle of PWM stage at nominal input (PFC output) voltage is:

\[
D_{MIN} = D_{MAX} \frac{V_{ROUT}_{MIN}}{V_{ROUT}} = 0.45 \frac{310}{389} = 0.36
\]

The sum of two normalize output current is:

\[
I_{SUM} = \frac{P_{O1} + P_{O2}}{V_{O1}} = \frac{243}{5} = 48.6\, A
\]

Assuming 16% p-p ripple current in I\(_{SUM}\), the inductor for the first output is obtained as:

\[
L_1 = \frac{V_{O1}(V_{O1}+V_{F1})}{f_{SW}(P_{O1}+P_{O2})} \frac{\Delta I_{SUM}}{I_{SUM}} (1 - D_{MIN})
\]

\[
= \frac{5(5+0.45)}{65 \times 10^3 (5 \times 9 + 12 \times 16.5) \times 0.16} (1-0.36) = 6.9\, uH
\]

Then, the ripple current for each output is given as:

\[
\frac{\Delta I_{O1}}{I_{O1}} = \frac{\Delta I_{SUM}}{2} \frac{1}{I_{O1}} = \frac{48.6 \times 0.16}{9} \frac{1}{9} = 43\%
\]

\[
\frac{\Delta I_{O2}}{I_{O2}} = \frac{\Delta I_{SUM}}{2} \frac{N_{S1}}{N_{S2}} \frac{1}{I_{O2}} = \frac{48.6 \times 0.16}{2} \frac{3}{7} \frac{1}{16.5} = 10\%
\]
**[STEP-12] PWM Ramp Circuit Design**

For voltage-mode operation, the RAMP pin can be connected to a DC voltage through a resistor. When it is connected to the input of forward converter, ramp signal slope is automatically adjusted according to the input voltage providing line feed-forward operation. However, it can cause more power dissipation in the resistor. For better efficiency and lower standby power consumption, it is recommended to connect the RAMP pin to the VREF pin.

![Figure 22. Ramp Generation Circuit for PWM](image)

It is typical to use 470pF~1nF capacitor on the RAMP pin and to have the peak of the ramp signal around 2~3V.

The peak of the ramp voltage is given as:

\[
V_{RAMP,PK} = \frac{1}{C_{RAMP} \cdot R_{RAMP}} \cdot \frac{V_{REF}}{2f_{SW}}
\]  

(52)

**Design Example** Selecting \( C_{RAMP} \) and \( R_{RAMP} \) as 1nF and 22k, the PWM ramp voltage is obtained as:

\[
V_{RAMP,PK} = \frac{1}{1 \times 10^{-9} \cdot 22 \times 10^3} \cdot \frac{1}{2 \cdot 65 \times 10^7} = 2.6V
\]

**[STEP-13] Feedback Compensation Design for PWM Stage**

Figure 21 shows the typical cross regulation compensation circuit configuration for multi-output converters. The small signal characteristics of the compensation network is given as:

\[
\begin{align*}
\frac{\hat{V}_{FBPWM}}{V_{REF}} &= -\frac{R_{B}}{1 + s/\omega_{CP}} \left( \frac{1 + s/\omega_{C21}}{R_{OS1} R_{D} C_{F} s} \hat{V}_{O1} + \frac{1 + s/\omega_{C22}}{R_{OS2} R_{D} C_{F} s} \hat{V}_{O2} \right)
\end{align*}
\]  

(53)

where:

\[
\begin{align*}
\omega_{C1} &= \frac{1}{(R_{B1} / R_{B2}) C_{R}} \\
\omega_{C21} &= \frac{1}{R_{F} C_{F}} \\
\omega_{C22} &= \frac{1}{(R_{F} + R_{OS2}) C_{F}}
\end{align*}
\]  

(54)

![Figure 23. Feedback Compensation Circuit for PWM Stage](image)

The small signal equivalent circuit for control-to-output transfer function of the PWM power stage can be simplified as shown in Figure 24. The transfer function is fourth-order system because additional LC filters are used to meet the output voltage ripple specification. Therefore, it is recommended to use engineering software, such as PSPICE or Mathlab, to design the feedback loop.

![Figure 24. Simplified Small Signal Equivalent Circuit for Control-to-Output Transfer Function](image)
Design Summary

<table>
<thead>
<tr>
<th>Application</th>
<th>Output Power</th>
<th>Input Voltage</th>
<th>Output Voltage / Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATX Power</td>
<td>300W</td>
<td>85~264VAC</td>
<td>12V/16.5A ; 5V/9A ; -12V/0.8A ; 3.3V/13.5A</td>
</tr>
</tbody>
</table>

Features

- Meets 80+ specification
- FAN4800A fully pin-to-pin compatible with ML4800 and FAN4800 (needs few parts modify)
- Switch-charge technique of gain modulator can provide better PF and lower THD
- Leading and trailing modulation technique for reduce output ripple
- Protections: OVP (Over-Voltage Protection), UVP (Under-Voltage Protection), OLP (Open-Loop Protection), and maximum current limit

Figure 25. Final Schematic of Design Example
Figure 26. Forward Converter Transformer Structure

### Winding Specification

<table>
<thead>
<tr>
<th>No</th>
<th>Pin(s-f)</th>
<th>Wire</th>
<th>Turns</th>
<th>Winding Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>3-2</td>
<td>0.6Φ</td>
<td>37Ts</td>
<td>Solenoid Winding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insulation: Mylar Tape t = 0.03mm, 3 Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N2</td>
<td>8,9-10,11,12</td>
<td>Copper-Foil 10mil</td>
<td>3Ts</td>
<td>Copper-Foil Width 18mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insulation: Mylar Tape t = 0.03mm, 1 Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N3</td>
<td>13-8,9</td>
<td>1.0Φ*4</td>
<td>4Ts</td>
<td>Solenoid Winding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insulation: Mylar Tape t = 0.03mm, 1 Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N4</td>
<td>10,11,12-14</td>
<td>0.4Φ</td>
<td>6Ts</td>
<td>Solenoid Winding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insulation: Mylar Tape t = 0.03mm, 1 Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N5</td>
<td>2-6,7</td>
<td>0.6Φ</td>
<td>37Ts</td>
<td>Solenoid Winding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insulation: Mylar Tape t = 0.03mm, 3 Layers</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Core-ERL35
- Insulation: Mylar Tape t = 0.03mm, 3 Layers
- Insulation: Copper-Foil Tape t = 0.05mm-pin1 Open Loop
- Insulation: Mylar Tape t = 0.03mm, 3 Layers

Core: ERL35 (Ae=107 mm²)
Bobbin: ERL35
Inductance: 13mH
Appendix A

FAN480X Series Comparison Table of Relevant Parameters

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V_{DD} Maximum Rating</strong></td>
<td>20V</td>
<td>30V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>V_{DD} OVP</strong></td>
<td>17.9V/Clamp</td>
<td>28/Auto-Recover</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>V_{CC} UVLO</strong></td>
<td>10V/13V</td>
<td>9.3/11V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Two-Level PFC Output</strong></td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PFC Soft-Start</strong></td>
<td>NO</td>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Brownout</strong></td>
<td>NO</td>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PFC : PWM Frequency</strong></td>
<td>1 : 1</td>
<td>1 : 1</td>
<td>1 : 2</td>
<td>1 : 1</td>
<td>1 : 2</td>
</tr>
<tr>
<td><strong>Frequency Range</strong></td>
<td>68kHz~81kHz</td>
<td>50kHz~75kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Gate Clamp</strong></td>
<td>NO</td>
<td>16V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PFC Multiplier</strong></td>
<td>Traditional</td>
<td>Switching Charge</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>V_{nOK}</strong></td>
<td>2.25V/1.1V</td>
<td>2.40V/1.15V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PWM Maximum Duty</strong></td>
<td>42%~49%</td>
<td>49.5%~50%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Startup Current</strong></td>
<td>100μA</td>
<td>30μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Soft-Start Current</strong></td>
<td>20μA</td>
<td>10μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PWM Comparator Level Shift</strong></td>
<td>1.0V</td>
<td>1.5V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>R_{AC}</strong></td>
<td>1~2MΩ</td>
<td>5~8 MΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

MOSFET and Diode Reference Specification

**PFC MOSFETs**

<table>
<thead>
<tr>
<th>Voltage Rating</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>500V</td>
<td>FQP13N50C, FQPF13N50C, FDP18N50, FDPF18N50, FDA18N50, FDP20N50(T), FDPF20N50(T)</td>
</tr>
<tr>
<td>600V</td>
<td>FCP11N60, FCPF11N60, FCP16N60, FCPF16N60, FCP18N60, FCP20N60S, FCPF20N60S, FCA20N60S, FCP20N60, FCPF20N60</td>
</tr>
</tbody>
</table>

**Boost Diodes**

<table>
<thead>
<tr>
<th>Voltage Rating</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td>FFP08H60S, FFPF10H60S, FFP08S60S, FFP08S60SN, BYC10600</td>
</tr>
</tbody>
</table>

**PWM MOSFETs**

<table>
<thead>
<tr>
<th>Voltage Rating</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>500V</td>
<td>FQP/PF9N50C, FQPF9N50C, FQP13N50C, FQPF13N50C, FQA13N50C, FDP18N50, FDPF18N50, FDP20N50(T), FDPF20N50(T)</td>
</tr>
<tr>
<td>600V</td>
<td>FCP11N60, FCPF11N60, FCP16N60, FCPF16N60, FCP18N60, FCP20N60S, FCPF20N60S, FCA20N60S, FCP20N60, FCPF20N60, FCA20N60</td>
</tr>
</tbody>
</table>
References

FAN480X — PFC/Forward PWM Controller Combo (FAN4800, FAN4801, FAN4802)

AN-6078SC — FAN480X PFC+PWM Combo Controller Application
AN-6004 — 500W Power Factor Corrected (PFC) Design with FAN4810
AN-6032 — FAN4800 Combo Controller Applications

AN-42030 — Theory and Application of the ML4821 Average Current Mode PFC Controller
AN-42009 — ML4824 Combo Controller Applications

ATX 300W 80+ Evaluation Board of FAN4800A+SG6520+FSQ0170